

METHOD FOR ERASING A MEMORY CELL

CROSS REFERENCE TO OTHER APPLICATIONS

[001] The present application is a continuation-in-part of US Patent Application *now Patent No. 6,643,181* 09/983,510, entitled "Method For Erasing A Memory Cell", assigned to the assignee of the present application, and claims priority therefrom.

FIELD OF THE INVENTION

[002] The present invention relates generally to erasing memory cells of non-volatile memory arrays, and particularly to methods for erasing a bit of a memory cell so as to reduce retention loss thereafter and increase reliability.

BACKGROUND OF THE INVENTION

[003] A well known type of non-volatile cell is a nitride, read only memory (NROM) cell, described in such patents as Applicant's US Patent 6,490,204, entitled "Programming And Erasing Methods For An NROM Array", and Applicant's US Patent 6,396,741, entitled "Programming Of Nonvolatile Memory Cells", the disclosures of which are incorporated herein by reference.

[004] Unlike a floating gate cell, the NROM cell has two separated and separately chargeable areas. Each chargeable area defines one bit. The separately chargeable areas are found within a nitride layer formed in an oxide-nitride-oxide (ONO) sandwich underneath a gate. When programming a bit, channel hot electrons are injected into the nitride layer. Programming an NROM cell may typically involve applying positive voltages to gate and drain terminals of the transistor, while the source may be floated.

[005] Erasing an NROM cell requires decreasing the threshold voltage of the cell. Erasing an NROM cell, which is done in the same source/drain direction as programming, typically involves applying a negative voltage to the gate and a positive voltage to the drain, while the source may be floated. The negative gate voltage creates holes in the